The ALU design is simulated using the ALU test bench

The test bench comprises of several different inputs for two variables and a case selection input to determine which operation has to be performed. The test bench then simulates these inputs on the ALU design and generates outputs in form of a wave. The simulation has been generated using the “xlinx vivado” platform

There are 8 different operations in the ALU simulated using the test bench starting from subtraction, addition, equality check, not equal to check, less than or equal to check, greater than check, left shift, right shift and arithmetic right shift.

The case selection input which determines the operation to be performed is represented by the variable opCode in the waveform. The value of opCode for each operation (in hexadecimal) is as follows

Subtraction - 0x11

Addition - 0x10

equality check - 0x20

not equal to check -0x21

less than or equal to check -0x22

greater than check -0x23

left shift -0x30

right shift -0x31

arithmetic right shift -0x32

These operations take 2 inputs represented by ‘a’ and ‘b’ .The output generated by them is then stored in the register variable ‘ ans1’ The N and Z outputs are flags which show weather the output ans1 is negative or not and zero or not respectively.